IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Thomas W. Williams et al.

Assignee: Synopsys, Inc.

Title: INTELLIGENT TEST VECTOR FORMATTING TO REDUCE TEST VECTOR SIZE AND ALLOW ENCRYPTION THEREOF FOR INTEGRATED CIRCUIT TESTING

Serial No.: 09/728,022 File Date: November 30, 2000

Examiner: John J. Tabone Jr. Art Unit: 2133

Docket No.: SYN-0174

Date: October 11, 2005

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DO NOT Enter 11/04/05

AMENDMENT IN RESPONSE TO THE FINAL OFFICE ACTION

Initial Comments

Claims 7-13 and 17-20 are pending in this application.

Claims 7-10, 13, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,444,716 (Jarwala). Claims 11, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jarwala in view of U.S. Patent 6,101,622 (Lesmeister).

No claims are amended herein.